

FIG. 1A Prior Art

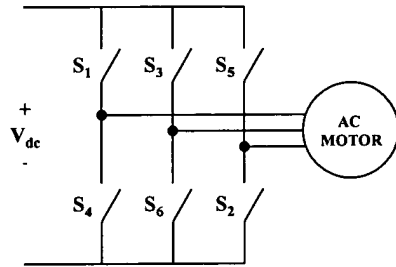


FIG. 1B Prior Art

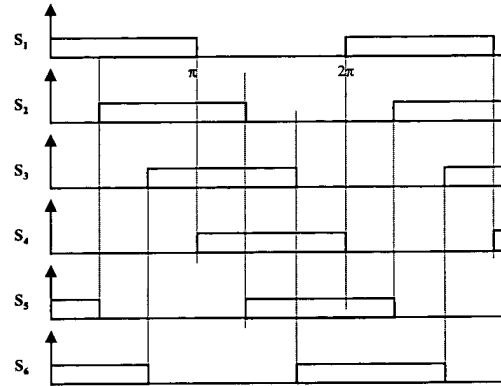


FIG. 1C Prior Art

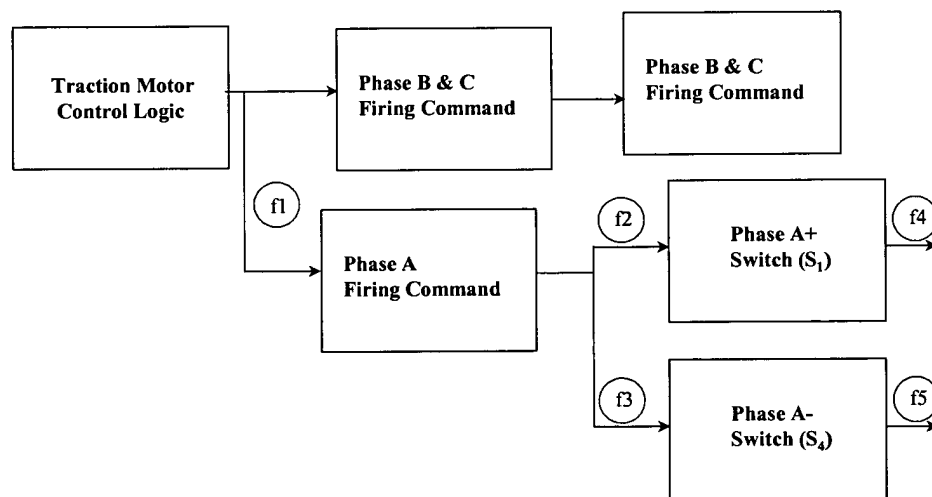


FIG. 2 Prior Art

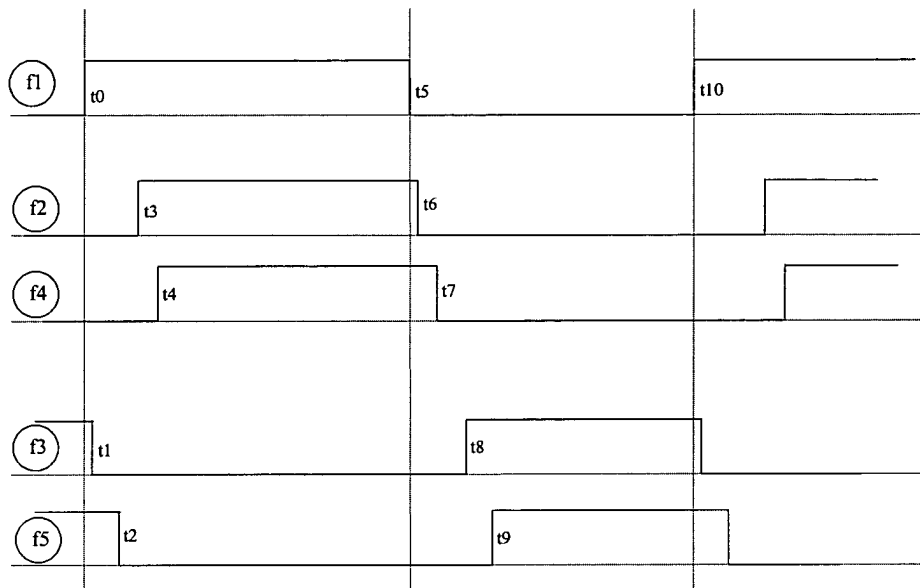


FIG. 3 Prior Art

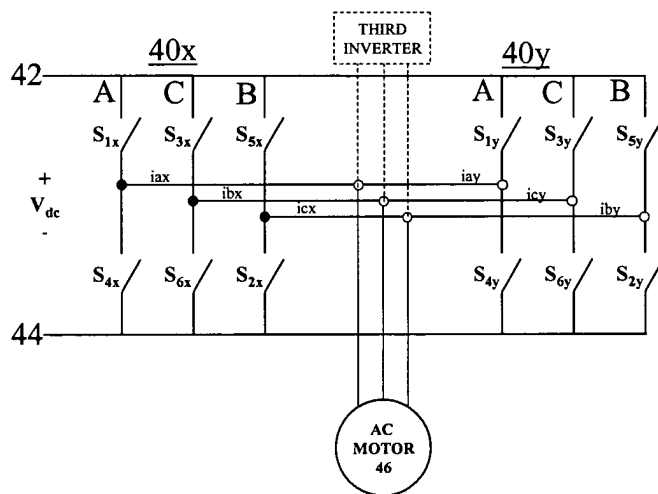


FIG. 4

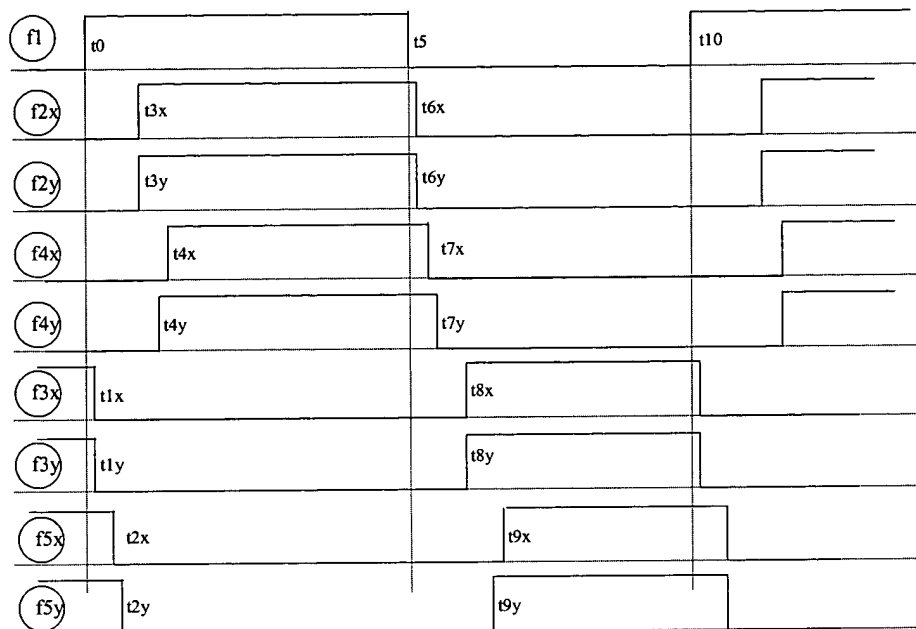


FIG. 5

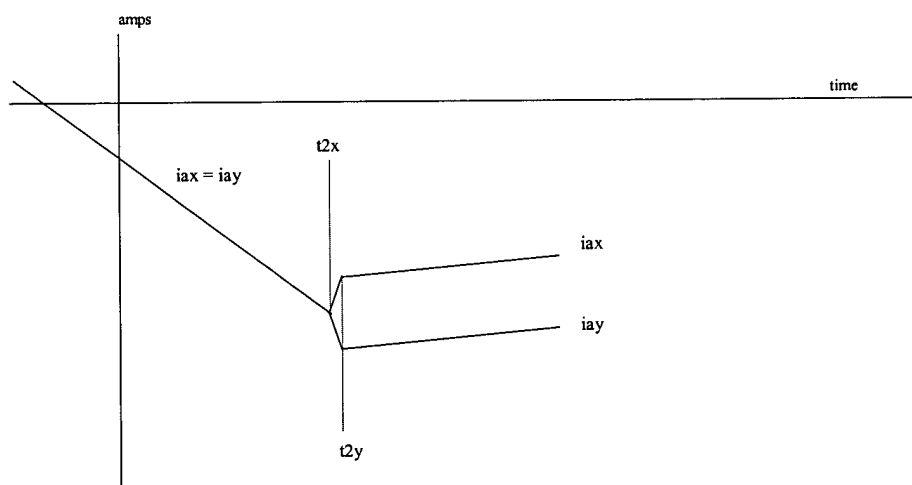


FIG. 6

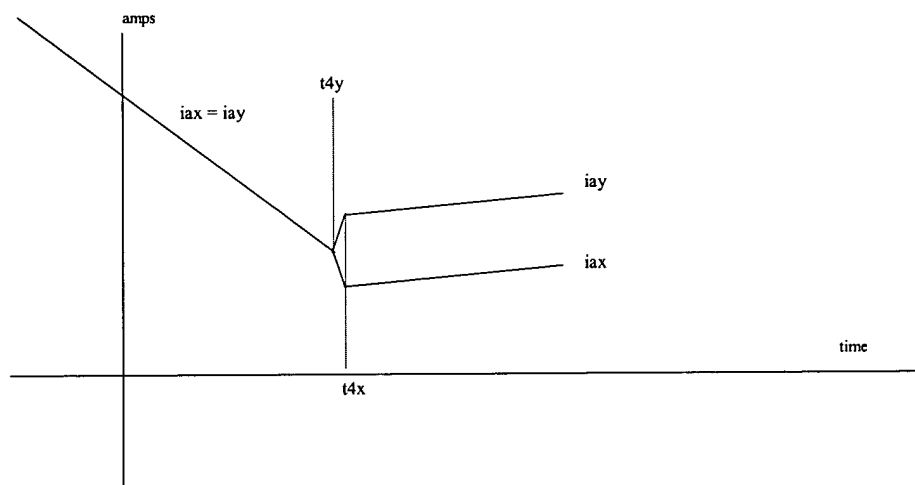


FIG. 7

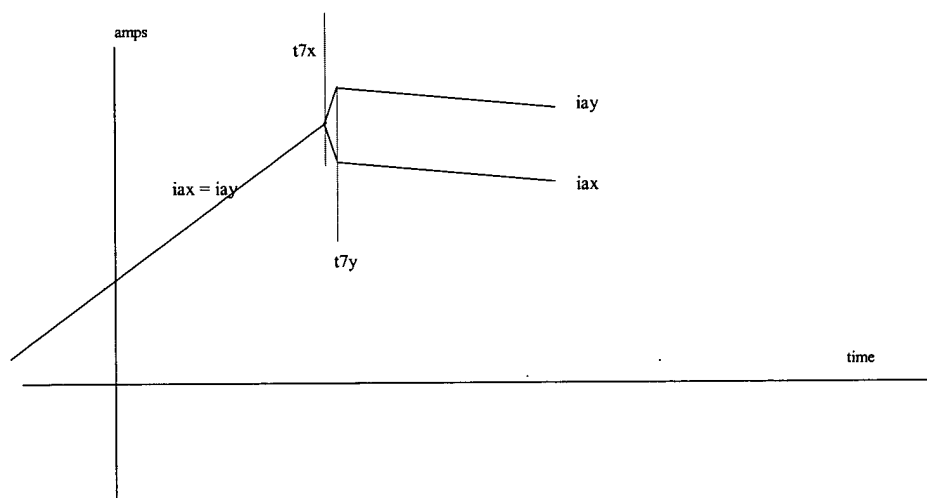


FIG. 8

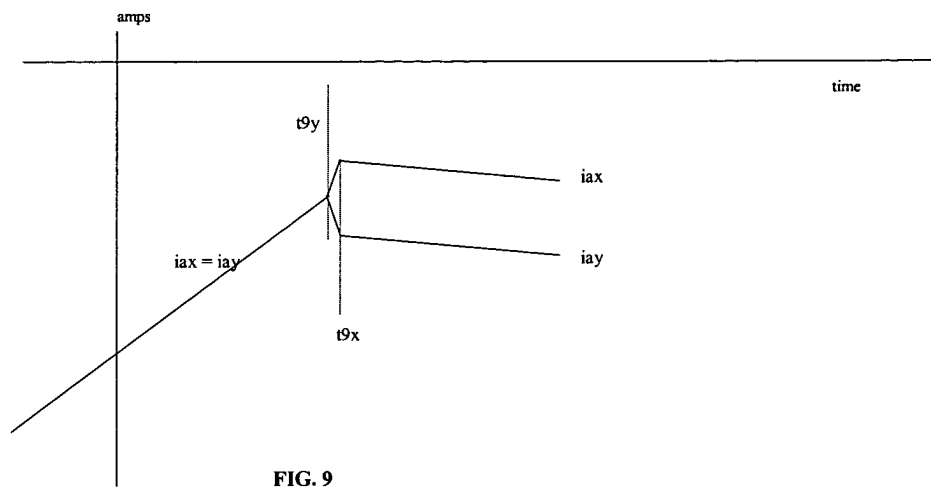


FIG. 9

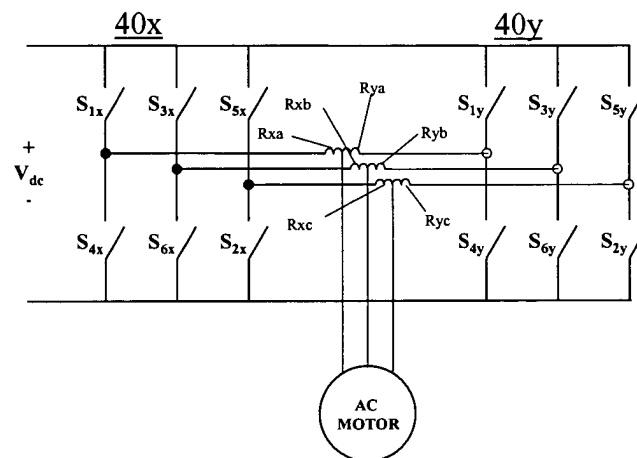


Fig. 10

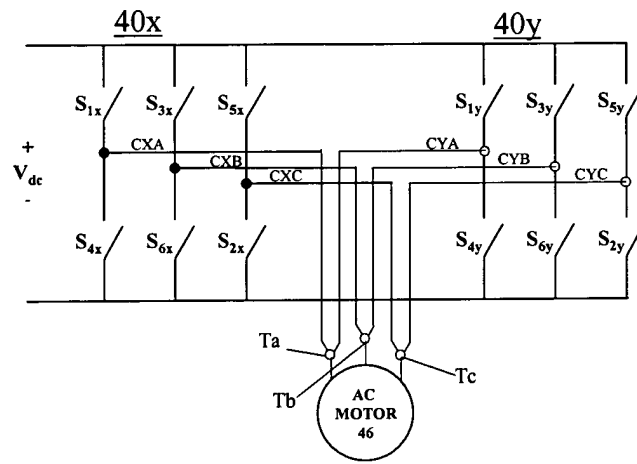


FIG. 11

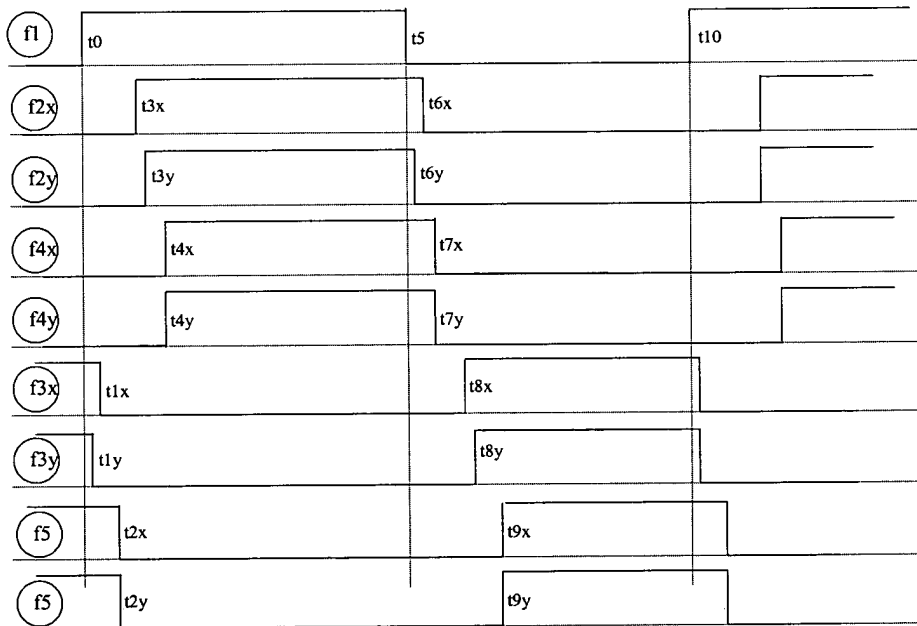


FIG. 12

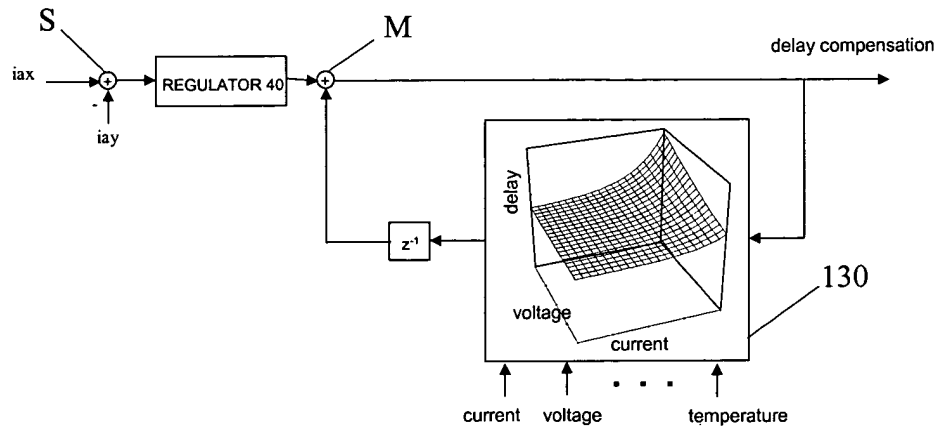


FIG. 13

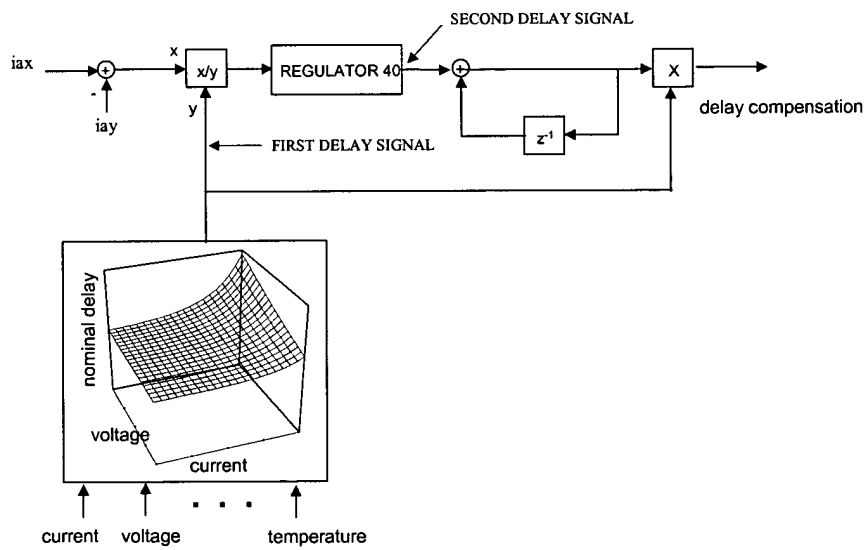


FIG. 14 Current equalizing regulator option 2

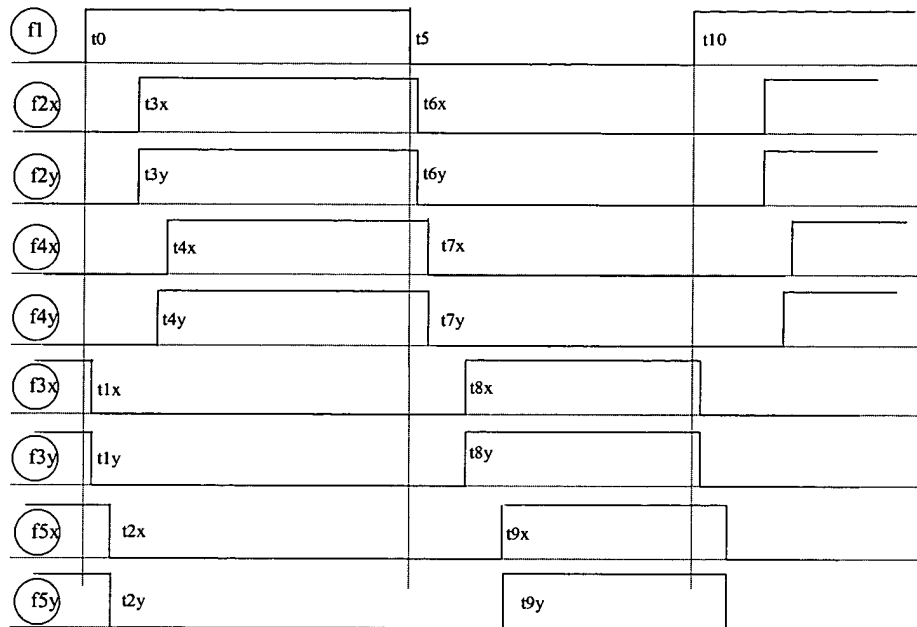


FIG. 15

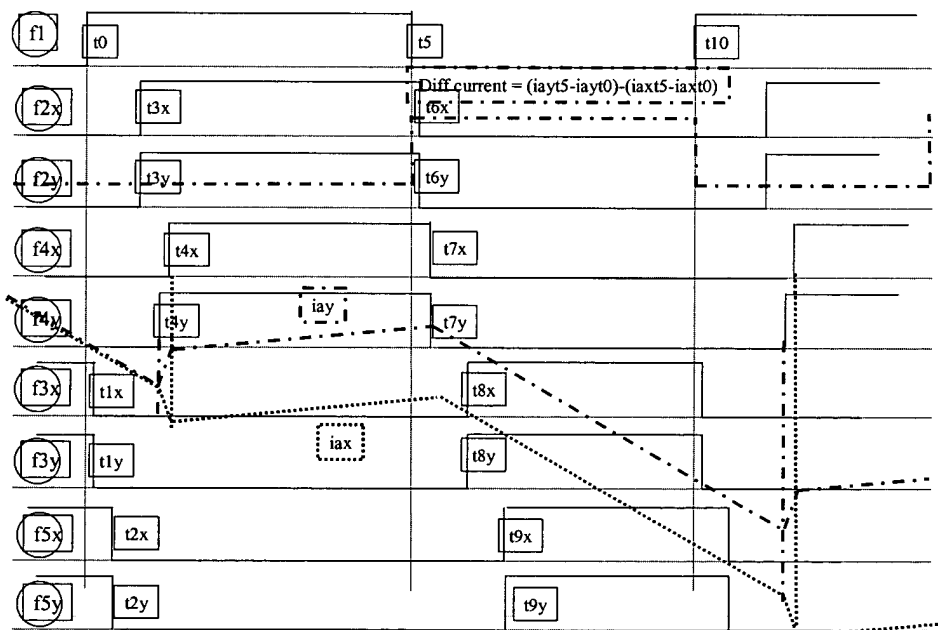


FIG. 16



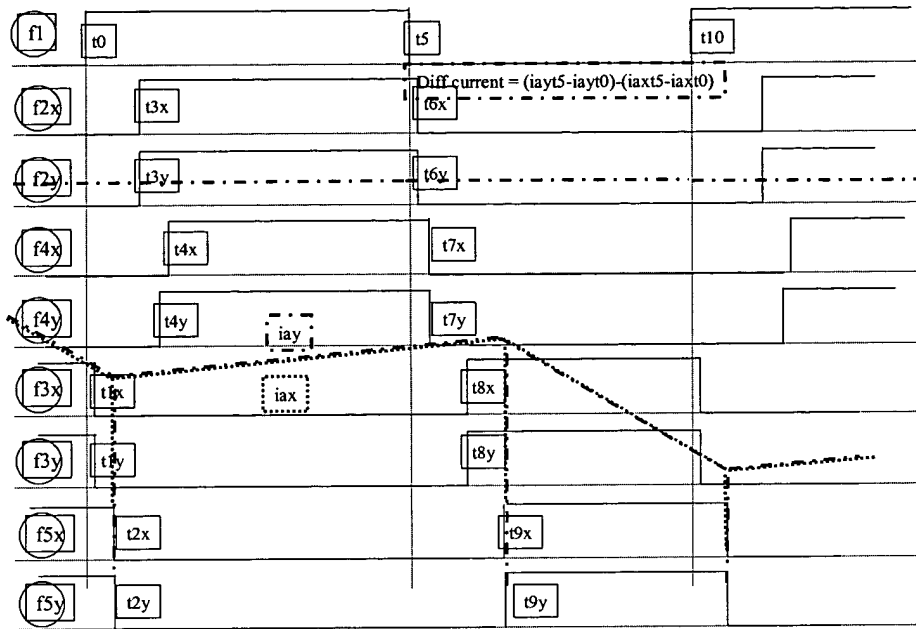


FIG. 17

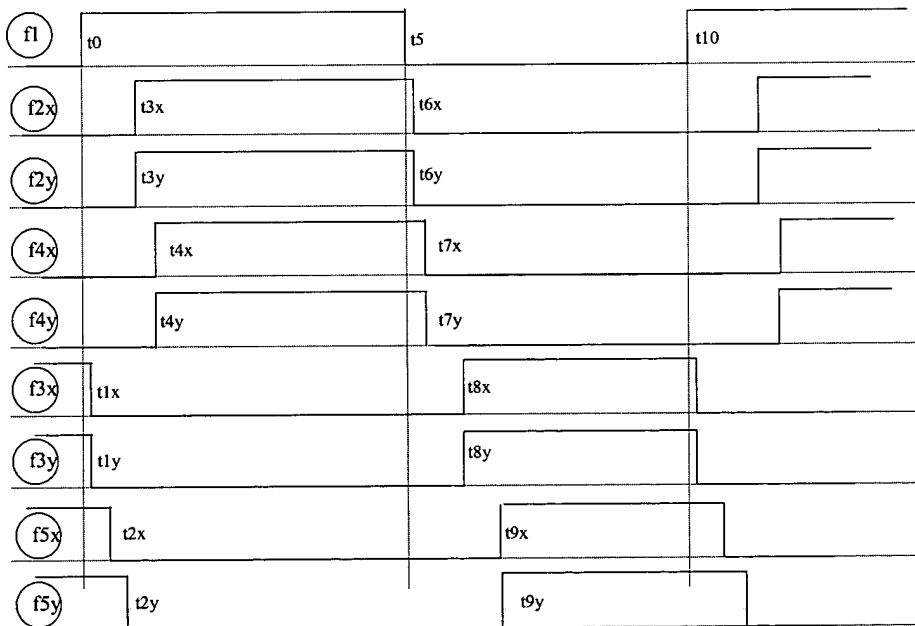
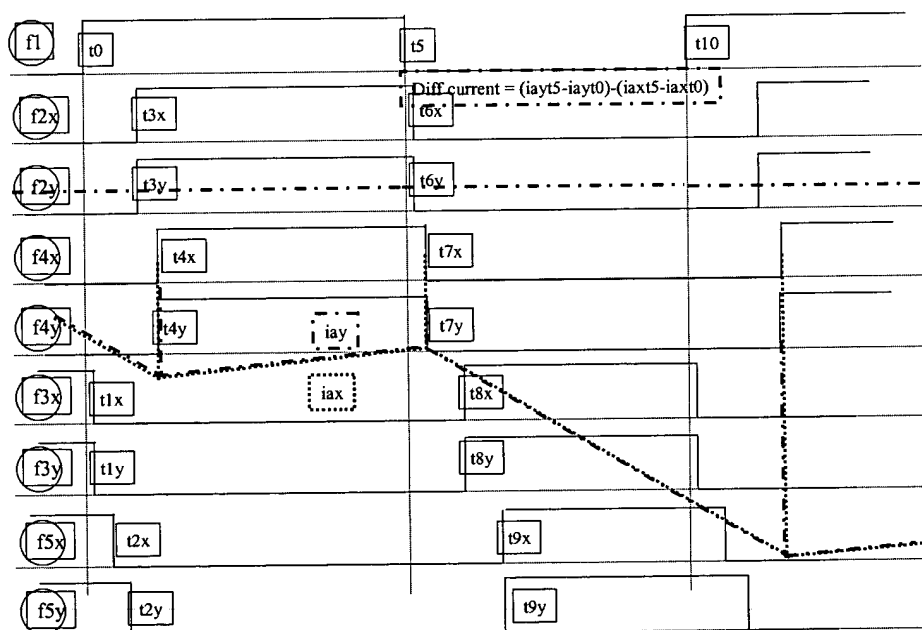
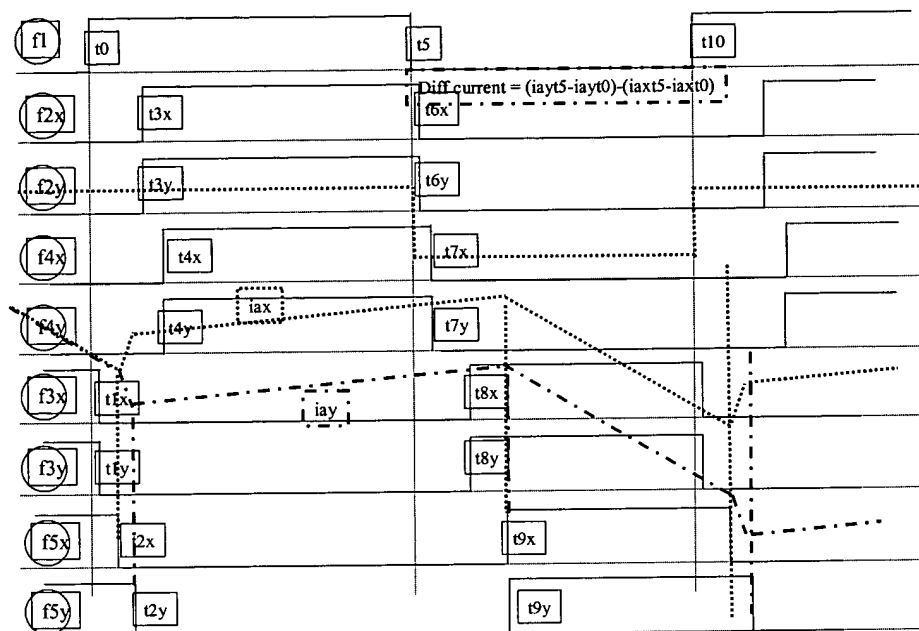


FIG. 18



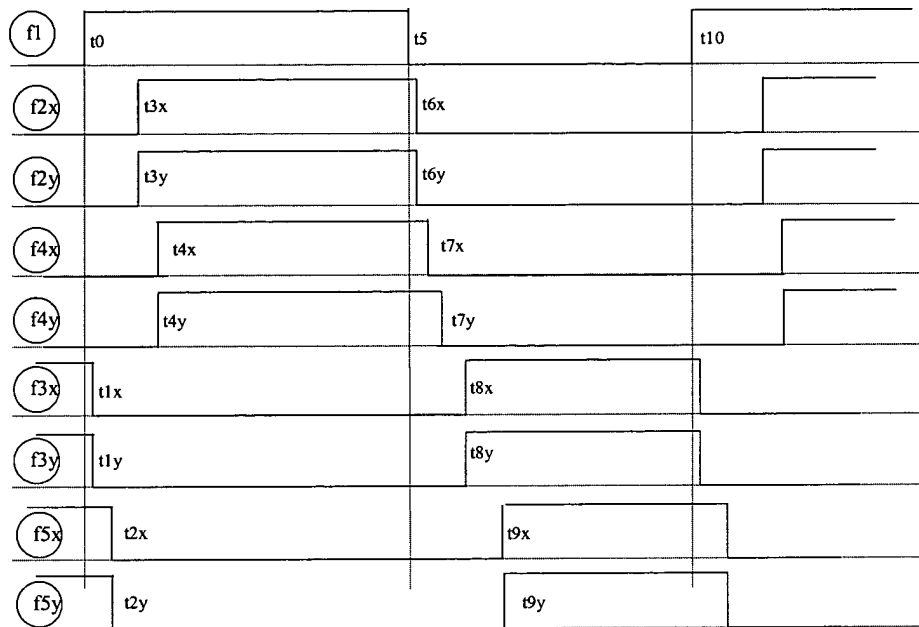


FIG. 21

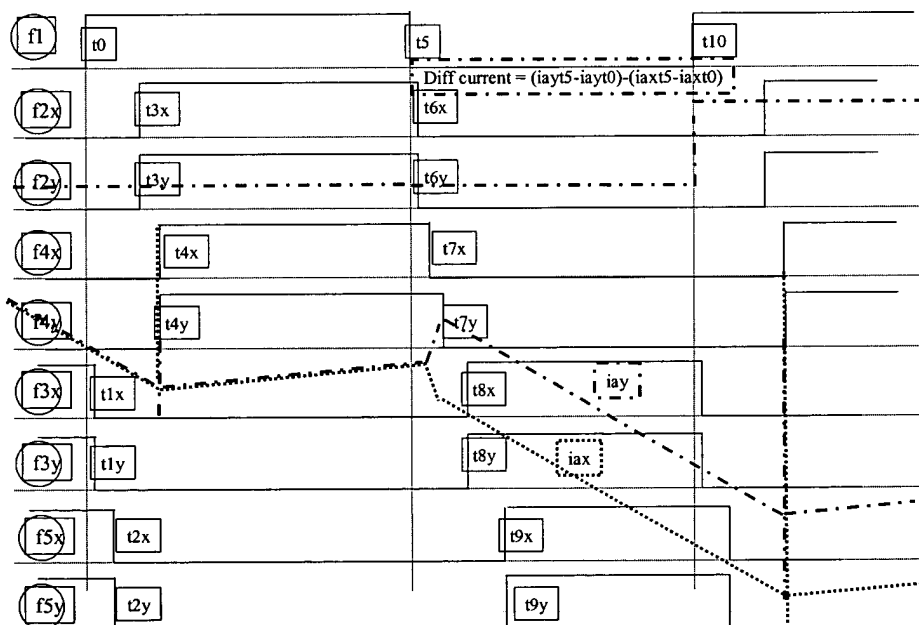


FIG. 22

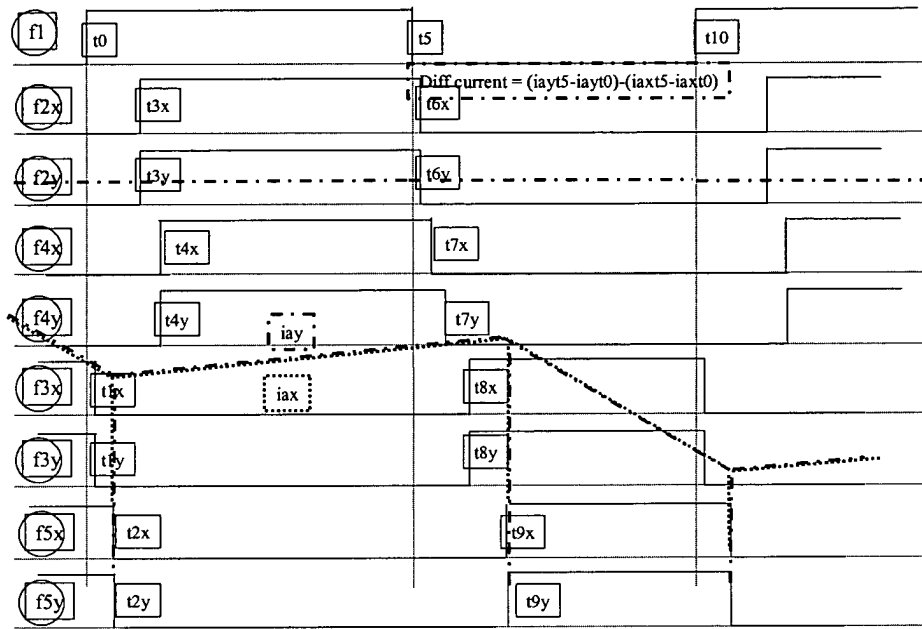


FIG. 23

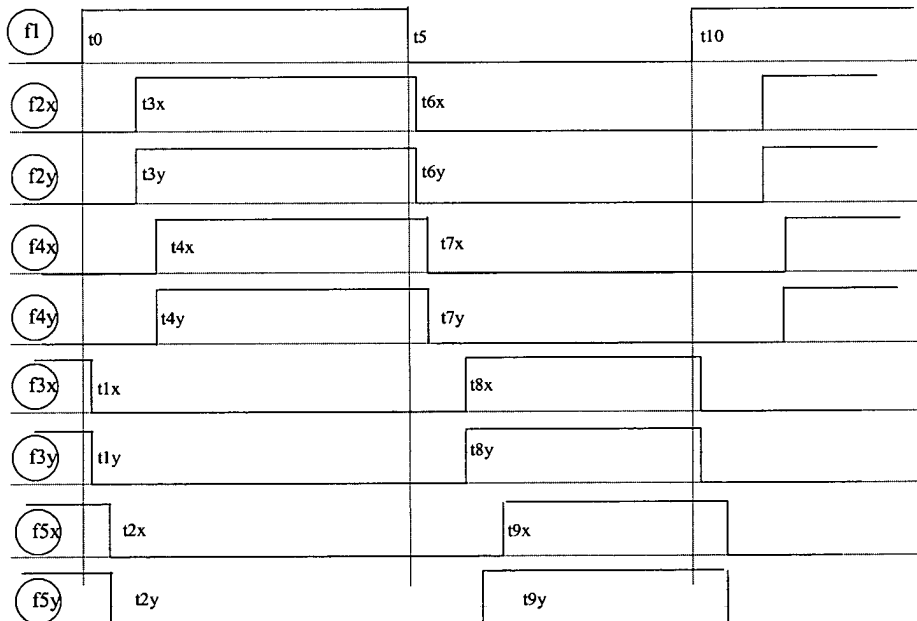


FIG. 24

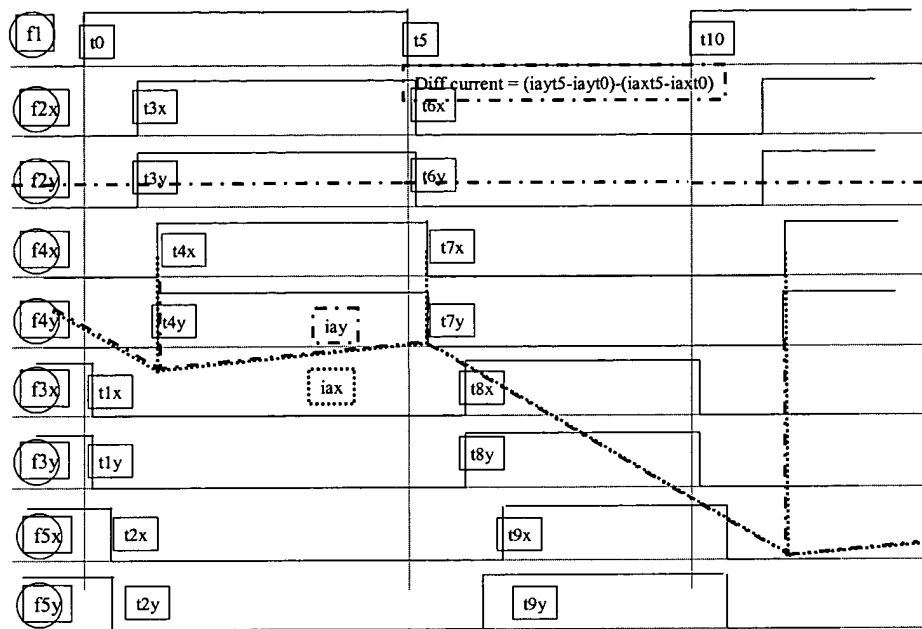


FIG. 25

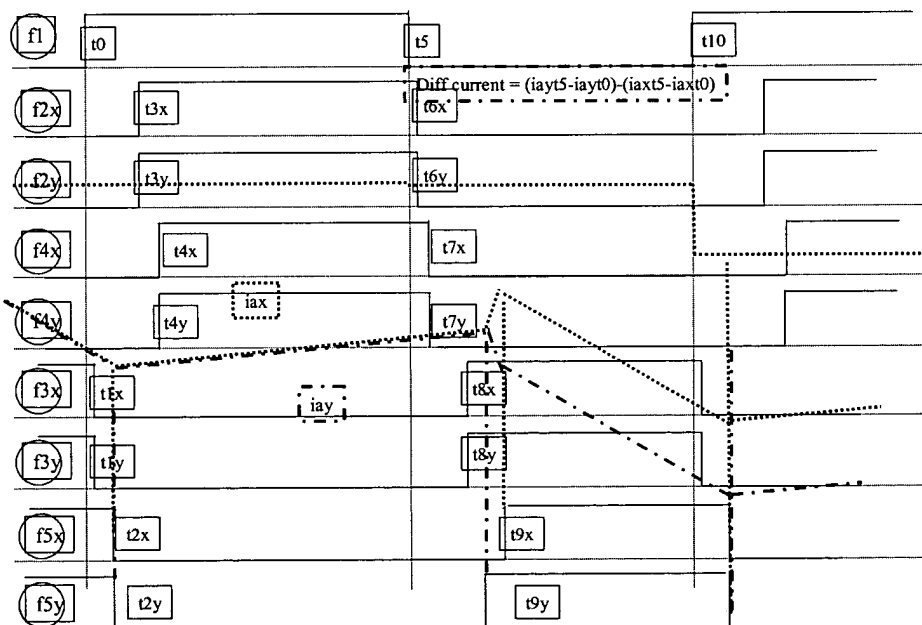


FIG. 26

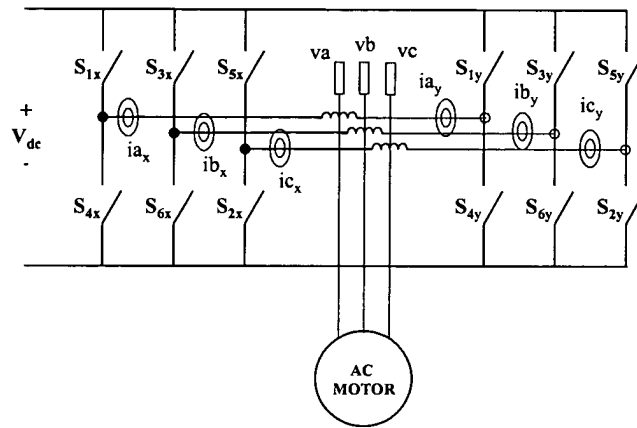


FIG. 27

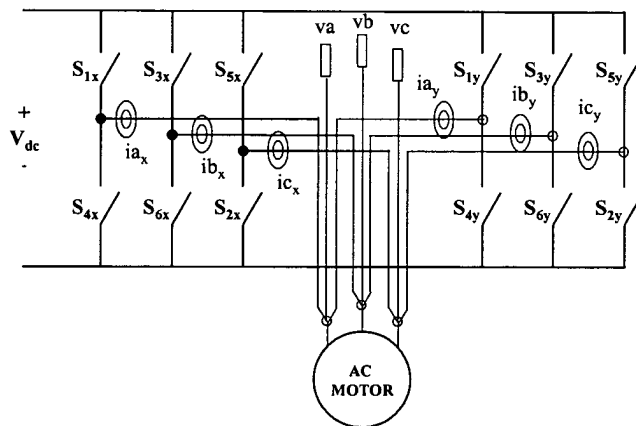


FIG. 28

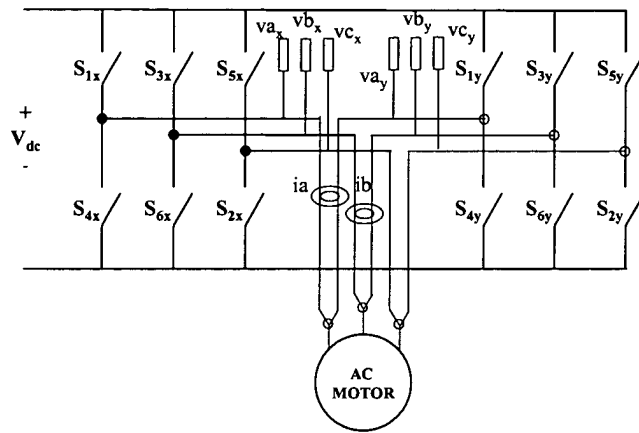


FIG. 29

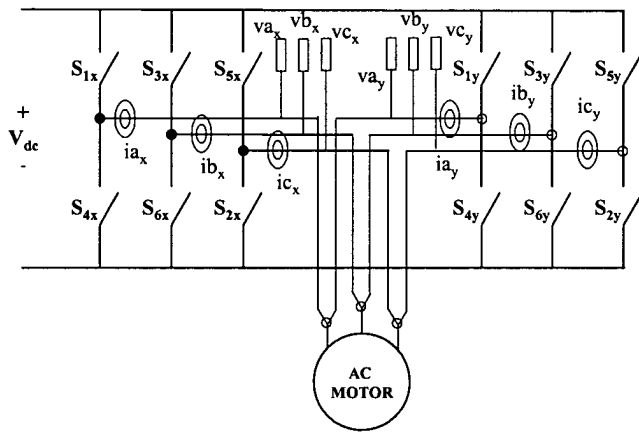


FIG. 30

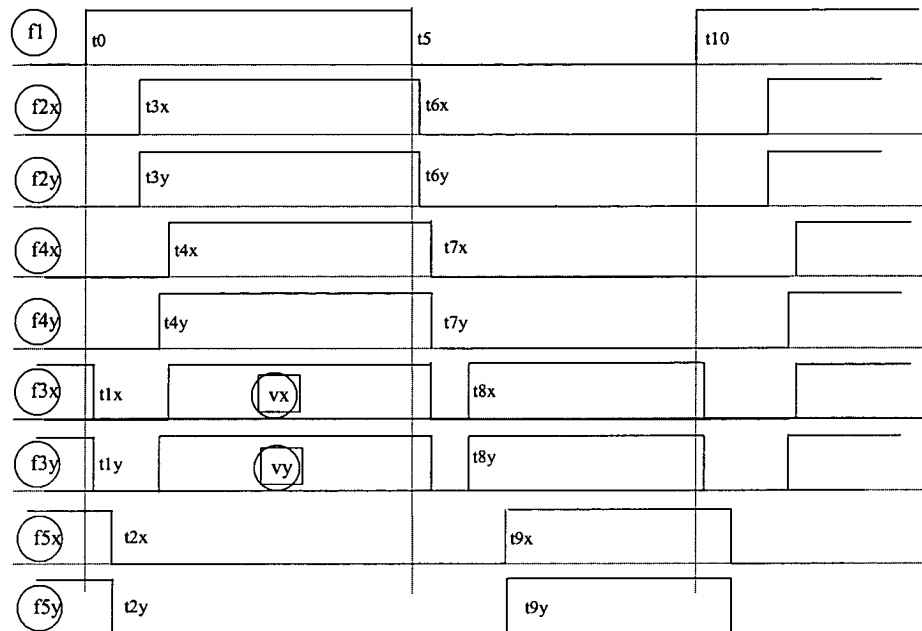


FIG. 31